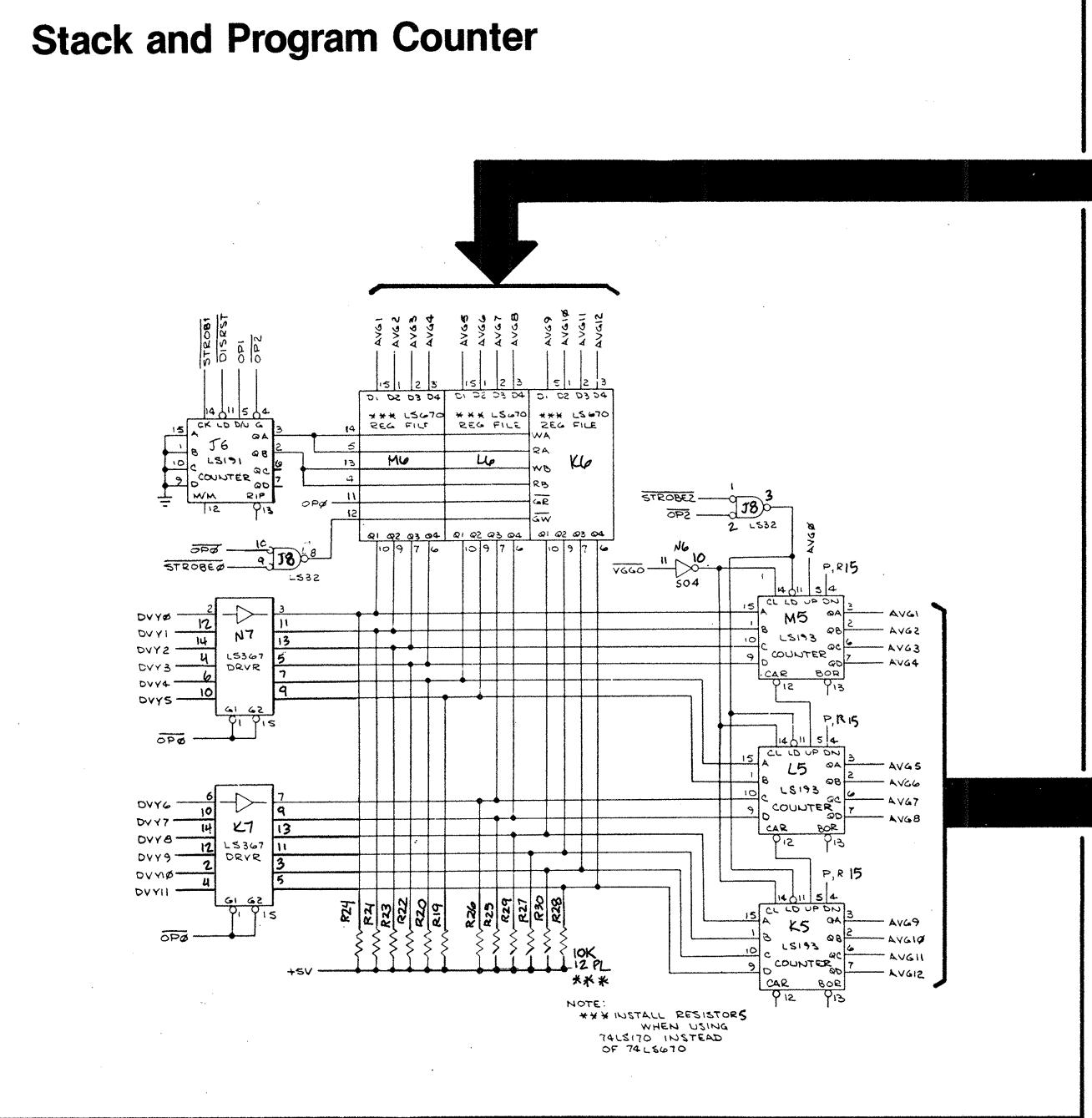
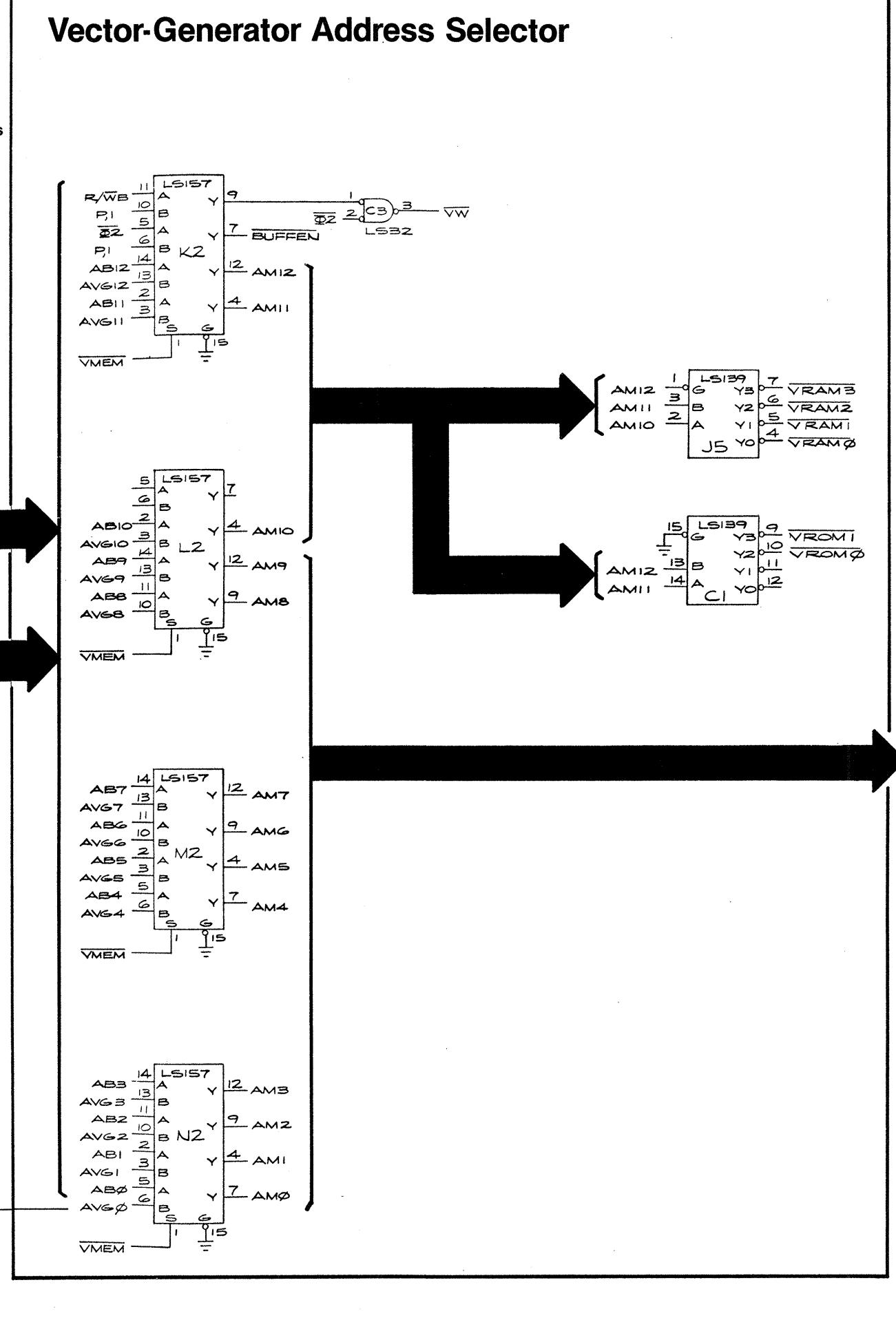


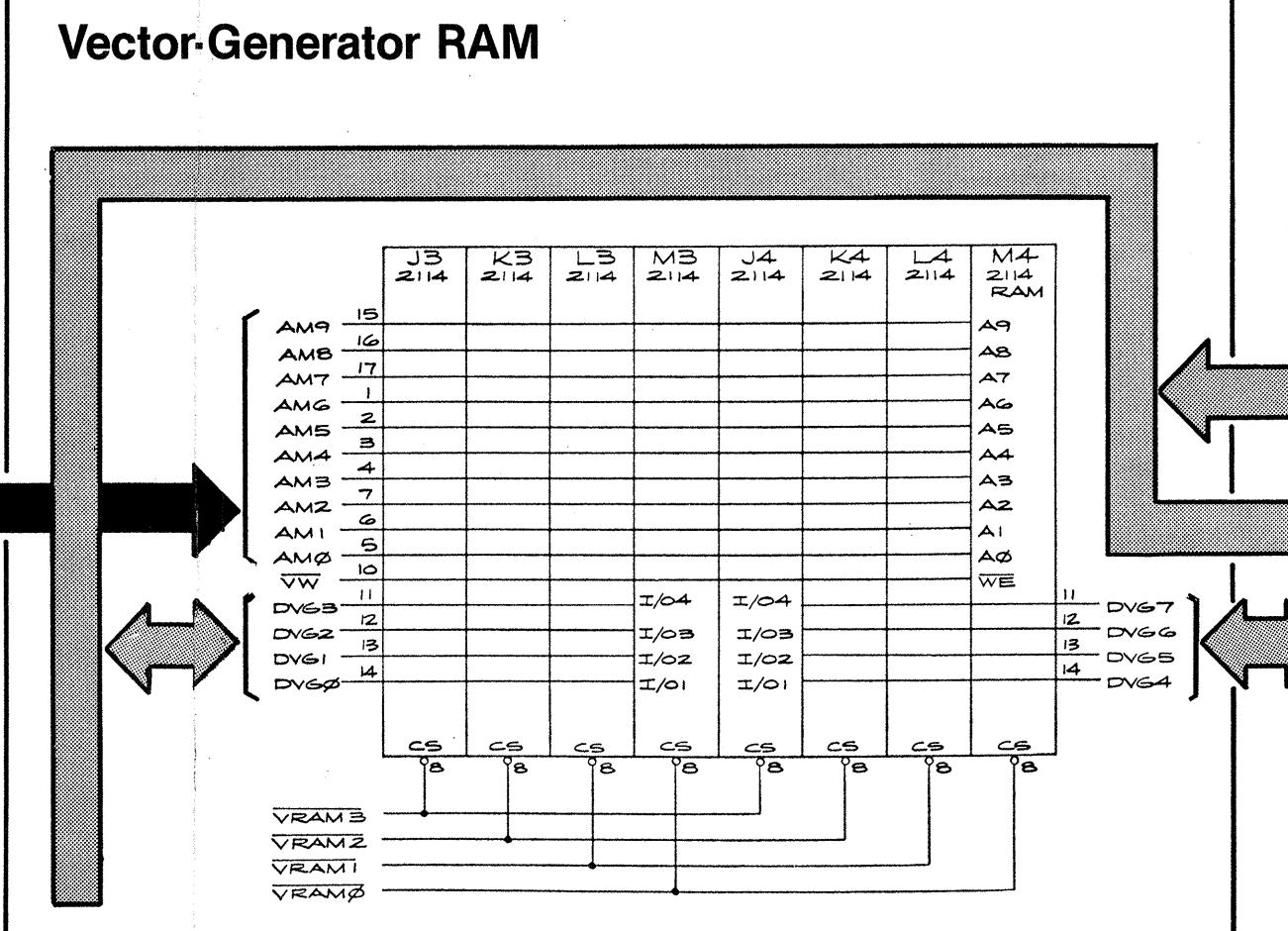
Stack and Program Counter



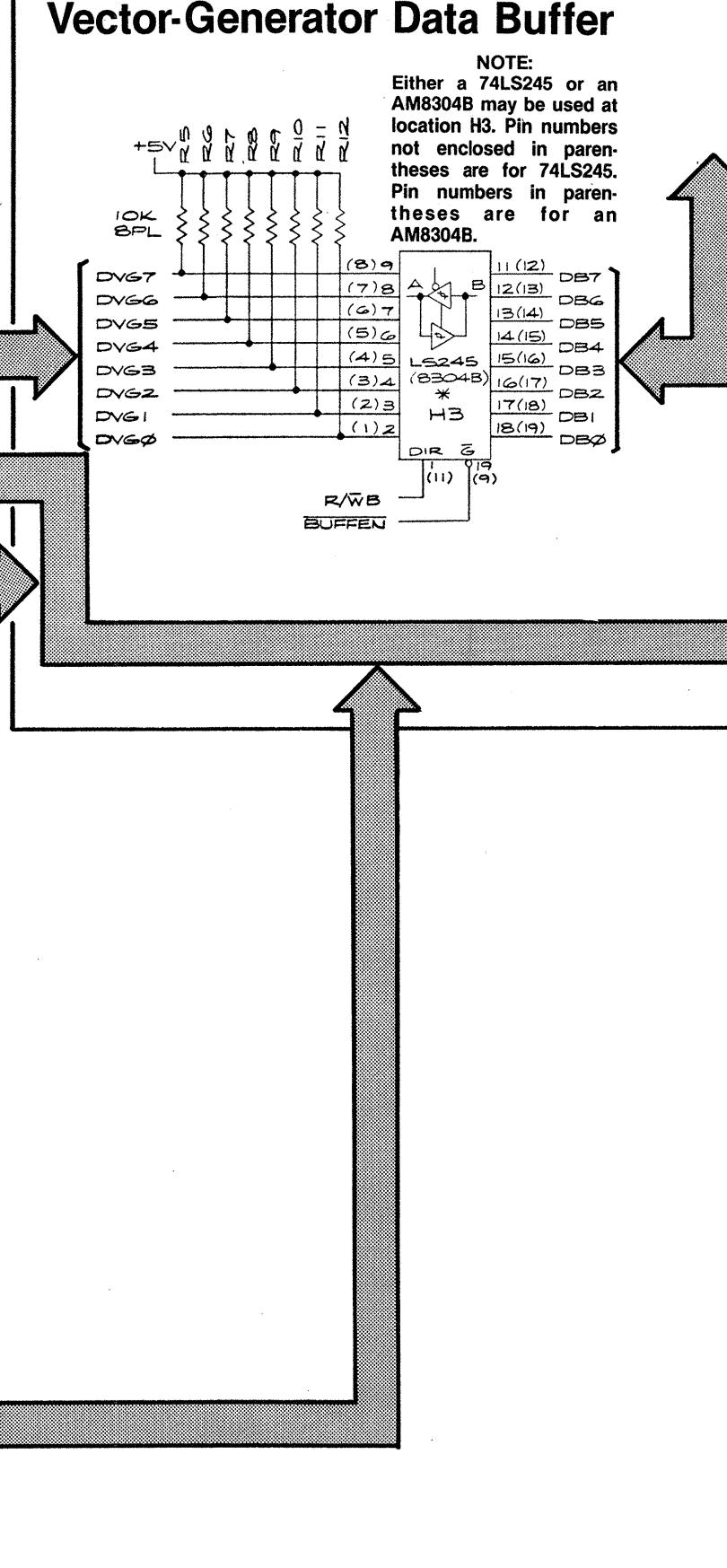
Vector-Generator Address Selector



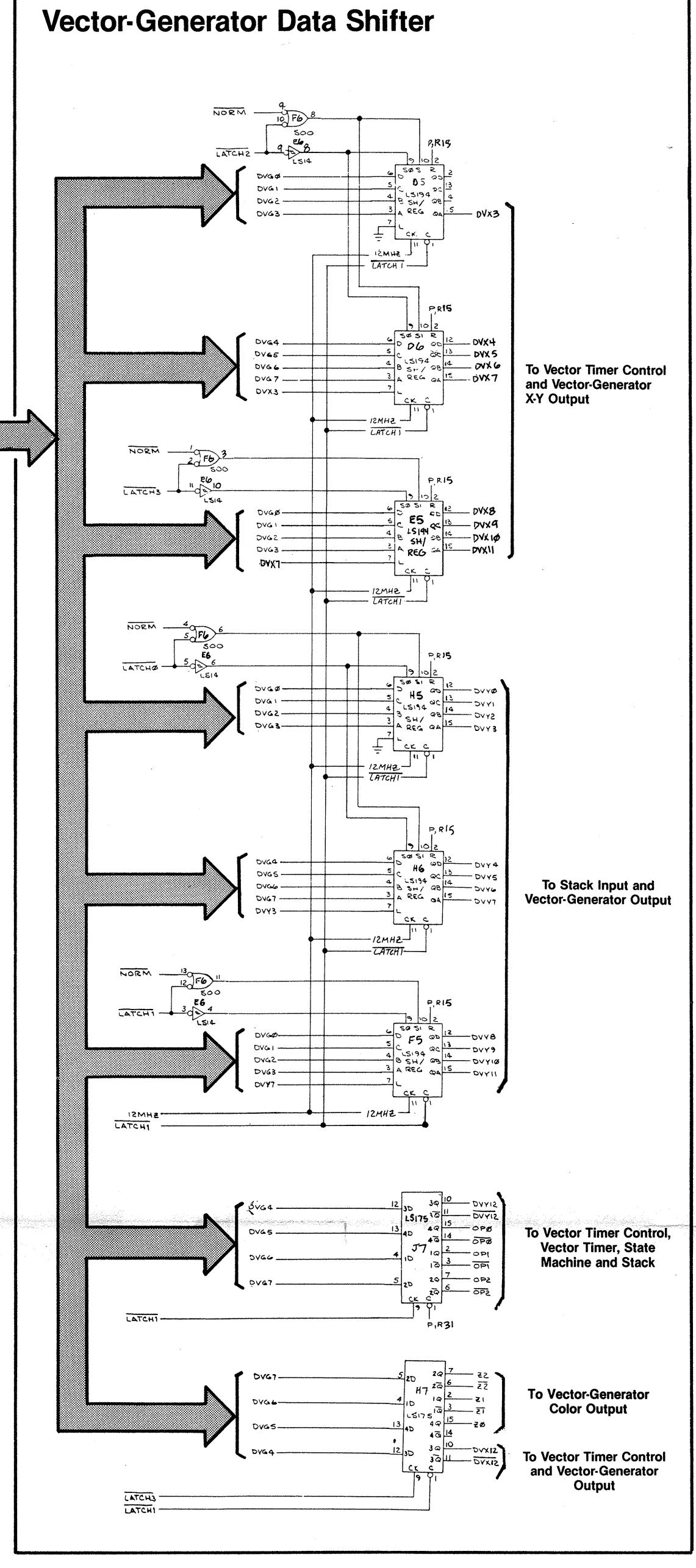
Vector-Generator RAM



Vector-Generator Data Buffer



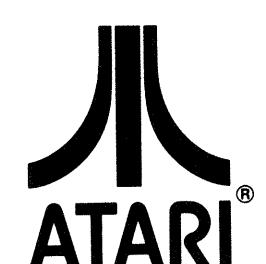
Vector-Generator Data Shifter



NOTE

- Indicates edge connector (J520)
- Indicates interconnect connector (J519)
- Indicates test point

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Sheet 3, Side A Tempest™

Vector-Generator Program Counter
Vector-Generator RAM
Vector-Generator ROM
Vector-Generator Data Shifter
Vector-Generator Data Buffer
Vector-Generator Address Selector
Vector-Generator Vector Timer
Vector-Generator State Machine
Section of 037383-01 & -02 B

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